

Supplementary information to: A Theory of Nested Cascading in Directed Logic

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I. CORRESPONDENCE OF THE HARDY AND SHAMIR'S GATES TO THE ONES USED IN THE PRESENT ARTICLE

Since the procedure of cascading in the article of Hardy and Shamir [1] is somewhat cumbersome, here we provide, for the sake of convenience, Figs. (1)-(2) where we show, side by side, their schemes, corresponding “straightened” schemes presented in our article, and their instantiations for the standalone gates. Note that by A' , A^{-1} is denoted in [1].

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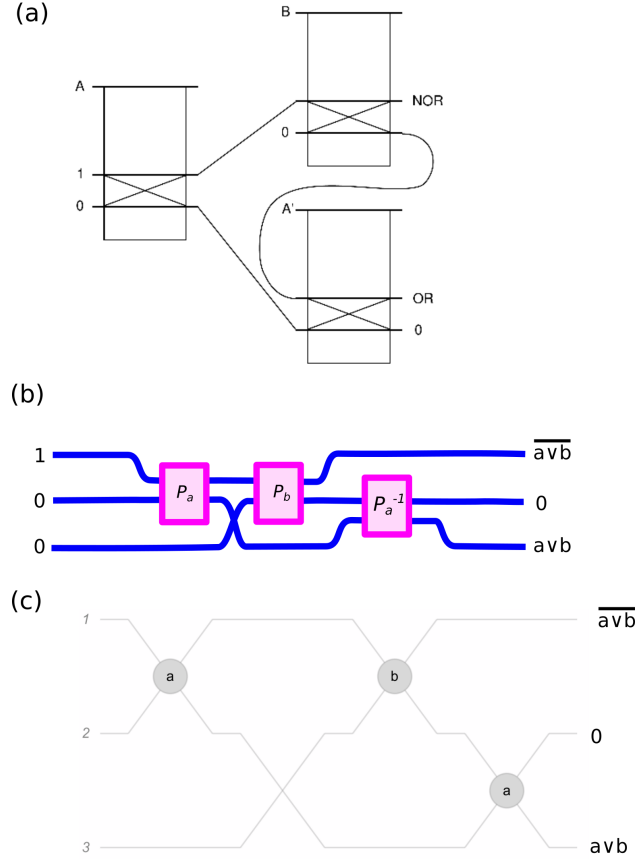


FIG. 1. Logical OR gate as presented in the article of Hardy and Shamir (a), in our paper in Fig.2b (b), and its substantiation in the form of a 1-gate circuit (c) (given also in Appendix A of the main article).

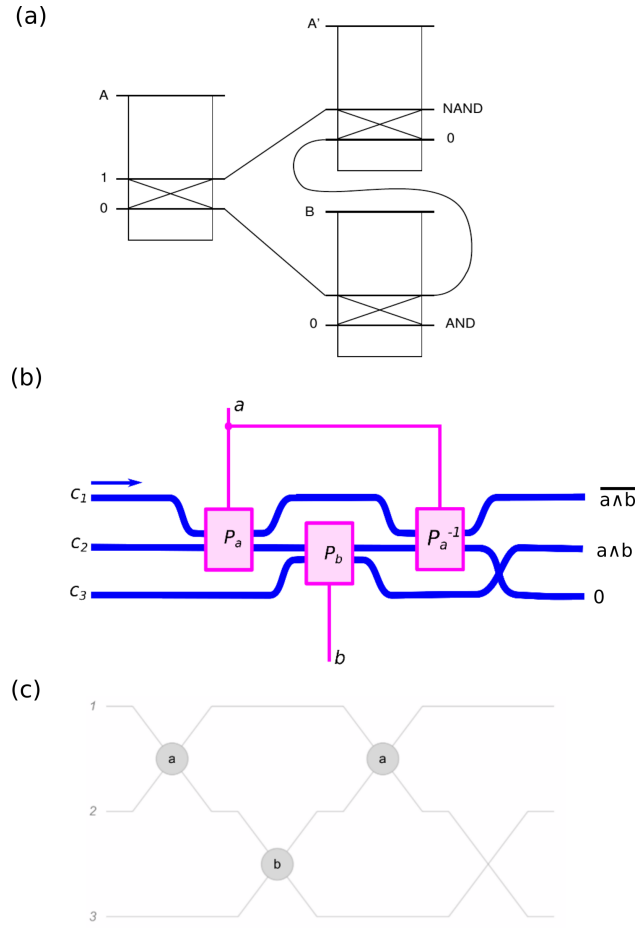


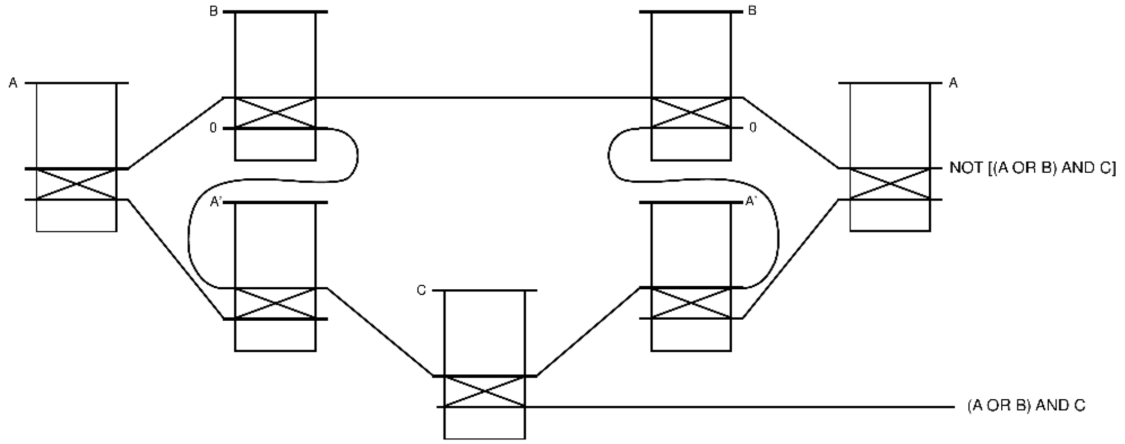
FIG. 2. Logical AND gate as presented in the article of Hardy and Shamir (a), in our paper in Fig.2a (b), and its substantiation in the form of a 1-gate circuit (c) (given also in Appendix A of the main article).

II. COMPARISON OF THE COMPOSITE GATE TOPOLOGY

In this section, we consider in detail the differences between the connection topology of our approach and that of Shamir and Hardy [1]. As an example, we consider the circuit implementing $(a \vee b) \wedge c$ (see Fig. 3). We see that the overall connectivity is very similar, but not identical. For instance, in Fig. 3(b), if we start from the leftmost A and assume $A = 1$, we arrive at A' . If we then assume $A' = 0$, we immediately reach the output of the circuit. In contrast, in Fig. 3(a), there is no path starting from the first element a that reaches the output after passing through only a single element. This shows that the connection topologies of the two schemes are, in general, not equivalent. On the other hand, the conditions $A = 1$ and $A' = 0$ can never occur simultaneously, since they refer to the same Boolean variable. Therefore, assuming that the circuit in Fig. 3(a) is correct, the nonequivalence between the two connection topologies can arise only along paths that are never realized.

[1] J. Hardy and J. Shamir, Optics inspired logic architecture, Opt. Express **15**, 150 (2007).

(a)



(b)

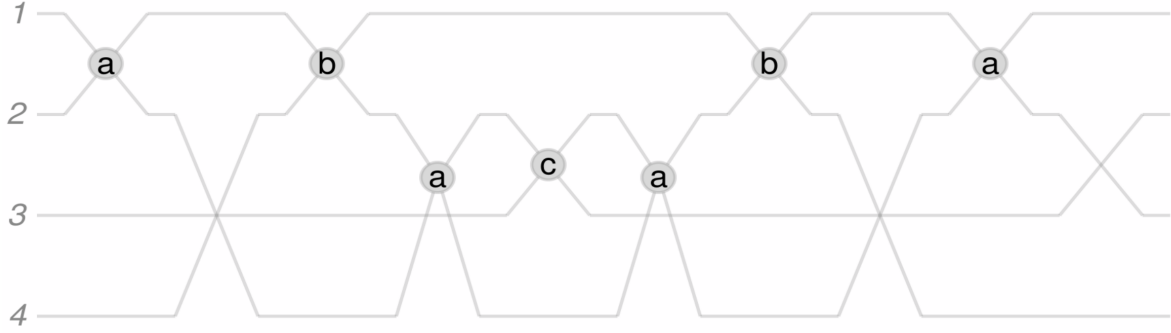


FIG. 3. DL circuit for $(a \vee b) \wedge c$ from Shamir and Hardy [1] (a) and obtained with our approach (b). The topologies are not completely equivalent (see text).