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A Low-Power RGC-Based CNTFET Transimpedance Amplifier for 40 Gbps Optical Receivers

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Abstract

In high-speed optical receivers, the transimpedance amplifier (TIA), as the first analog block, plays a critical role in converting the weak photodiode current into a processable voltage while providing the required bandwidth, low-noise, and low-power consumption. In this paper, a low-power TIA based on a regulated cascode (RGC) structure is designed for 40 Gbps optical applications using 32 nm carbon nanotube field-effect transistor (CNTFET) technology. In the proposed topology, the transconductance of the driver transistor is enhanced through gain boosting, while a diode-connected configuration is employed at the output node to reduce the effective output-node resistance, decrease the associated time constant, and extend the frequency response. Simulations based on the Stanford CNTFET model demonstrate that the proposed circuit achieves a transimpedance gain of 51.4 dBΩ, a −3 dB bandwidth of 28.3 GHz, an input-referred noise current of 5.3 pA/√Hz, and a power consumption of 368 μW. These results indicate that the proposed structure can be considered a suitable candidate for low-power TIA implementation in 40 Gbps optical receivers.

Keywords: Transimpedance Amplifier, Regulated Cascode, Low-Power, Optical Receiver, CNTFET.

Introduction

The rapid increase in data traffic, together with the widespread deployment of high-speed communication services, has created a growing need for optical links that can support high data rates, reliable signal recovery, and reduced power dissipation. In an optical receiver, the quality of data detection is strongly influenced by the analog front-end (AFE), which must process very small electrical signals generated from the received optical waveform. The photodiode first converts the incident optical signal into a weak photocurrent. This current must then be transformed into a voltage signal with sufficient amplitude and bandwidth, while limiting noise contribution and preserving the integrity of the received information. Accordingly, the TIA, as the first active amplification stage in the receiver chain, has a major impact on the achievable transimpedance gain, bandwidth, input-referred noise, and power consumption . ‘

At a data rate of 40 Gbps, the design of a TIA becomes particularly challenging because the key performance parameters are strongly interdependent. Increasing the transimpedance gain may restrict the bandwidth, strengthen the influence of parasitic capacitances, increase noise contribution, or require additional power dissipation. Therefore, establishing an appropriate compromise among gain, bandwidth, noise, and power consumption is a central design objective in high-speed optical receiver front-ends. In addition, technology scaling introduces further limitations, including reduced supply voltage and tighter voltage headroom constraints. These limitations make the input-stage design more sensitive to biasing and device-level nonidealities, and consequently make the circuit topology a decisive factor in determining the overall receiver performance ‘.

As shown in Figure 1, this work investigates the design of an RGC-based TIA implemented using CNTFET technology. The main objective is to enable 40 Gbps operation with low-power consumption while maintaining adequate front-end signal integrity. The proposed architecture is designed to improve the balance among transimpedance gain, bandwidth, input-referred noise, and power consumption, thereby providing a suitable circuit-level solution for high-speed optical receiver applications.

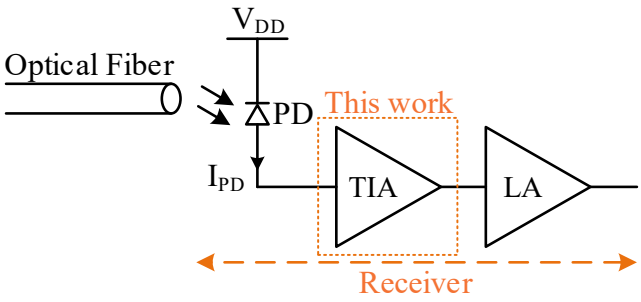


Figure 1. Block diagram of the analog front-end of the optical receiver .

Achieving a low bit error rate in high-speed optical receivers depends strongly on the design of the TIA, which serves as the first gain stage in the receiver front-end. This stage is required to convert the weak photocurrent generated by the photodiode into a voltage signal suitable for subsequent processing stages, while simultaneously meeting the required gain, bandwidth, and noise specifications. A major challenge in this context arises from the photodiode parasitic capacitance, which typically forms the dominant pole at the input node and thus limits the available bandwidth and degrades the overall receiver performance .

Accordingly, TIA design is governed by two main requirements. First, the relevant time constant must be minimized so that the dominant pole is shifted toward higher frequencies and the required bandwidth can be achieved. Second, the circuit must provide sufficient transimpedance gain to amplify small input currents without compromising signal detection quality [5]–[9]. For this reason, the design of TIAs that simultaneously exhibit low-power consumption, low-noise, and wide bandwidth has become a key issue in the development of optical receiver front-ends.

To address these requirements, several circuit topologies have been investigated, each offering a different balance among gain, bandwidth, noise, implementation complexity, and power consumption. The common-gate (CG) topology is structurally simple; however, its high-frequency performance can be constrained by input-impedance considerations and parasitic effects. By contrast, the RGC topology provides low input impedance, a suitable output-voltage swing, and high output impedance, making it a viable choice for high-speed receiver applications . Accordingly, this topology is adopted in the present work as the basis of the proposed TIA. Inverter-based structures are also of interest because they can provide high transconductance together with low input impedance, although their bandwidth may become limited under certain operating conditions. Moreover, cascaded inverter-based structures can improve gain and frequency response, but this improvement is often obtained at the cost of higher power consumption .

The choice of topology ultimately depends on the design targets of the intended application, including bandwidth, noise, power consumption, and supply voltage constraints. In high-speed receivers, the required TIA bandwidth is often estimated to be approximately 70% of the data rate . To satisfy this requirement, a range of bandwidth-extension methods has been reported. Among these methods, diode-connected and resistor-feedback techniques enhance the bandwidth by introducing an appropriate small-signal resistance at the node of interest, whereas the active-inductor approach extends the frequency response by generating an active inductance at the output node and establishing resonance with the load capacitance near the −3 dB cutoff frequency ‹.

Because this work also aims to reduce power consumption and avoid the use of passive elements, the diode-connected approach is selected to realize the desired frequency response. Based on this design strategy, this paper presents an RGC-based TIA implemented solely with active devices in order to reduce chip area, simplify circuit realization, and improve both frequency response and power consumption. In addition, a pass transistor and the diode-connected technique are incorporated into the proposed structure to further improve circuit performance.

As semiconductor devices continue to scale toward nanometer dimensions, conventional MOSFET technology faces increasingly severe physical and process-related constraints, including short-channel effects, leakage current, intensified electric fields, lithographic limitations, and quantum-confinement effects . Within this context, CNTFET technology has attracted considerable attention as a potential device platform for next-generation nanoelectronic circuits. This interest is primarily associated with the intrinsic electrical and material properties of carbon nanotubes, including

enhanced electrostatic control by the gate, high carrier mobility, comparable transport characteristics in n-type and p-type CNTFETs, the possibility of near-ballistic carrier transport, high transconductance, a large on/off current ratio, favorable thermal conductivity, and threshold-voltage tunability .

Despite these advantages, several practical challenges continue to limit the large-scale deployment of CNTFET-based circuits. These challenges include the complexity of fabrication processes, sensitivity to nanotube defects, difficulties in controlling structural and geometrical variations, and unresolved issues associated with very-large-scale integration (VLSI). Nevertheless, the operational resemblance between CNTFETs and MOSFETs, together with their partial compatibility with MOSFET process flows, provides an opportunity to exploit established circuit-design methodologies and fabrication infrastructures . Consequently, CNTFET technology represents a technically relevant candidate for high-speed integrated circuits with low-power consumption, including optical TIAs.

The remainder of this paper is organized as follows. The section entitled “Proposed Circuit Architecture and Design” first reviews the conventional RGC-based TIA topology and then presents the proposed CNTFET-based architecture. In this section, the effects of the pass-transistor and diode-connected configurations on the transimpedance gain, frequency poles, bandwidth, and input-referred noise are examined using the small-signal model. The section entitled “Simulation Results” reports the main simulation outcomes, including the key performance metrics, eye diagrams at 40 Gbps, Monte Carlo analysis, supply voltage sensitivity, and comparison with previously reported designs. Finally, the main conclusions are summarized in the section entitled “Conclusion”.

Proposed Circuit Architecture and Design

Conventional RGC-based TIA Topology

In TIAs, the CG configuration is widely employed to receive the photodiode current because its low input resistance facilitates efficient current transfer and reduces signal attenuation at the input. By incorporating a gain-boosting stage, typically implemented as a common-source (CS) amplifier, into the CG structure, the RGC topology is formed. As shown in Figure 2, this configuration increases the effective transconductance of the driver transistor, thereby reducing the input impedance beyond that of a conventional CG stage and creating more favorable conditions for bandwidth enhancement. In addition, the single-stage nature of this architecture simplifies the design and reduces the need for complex frequency-compensation schemes .

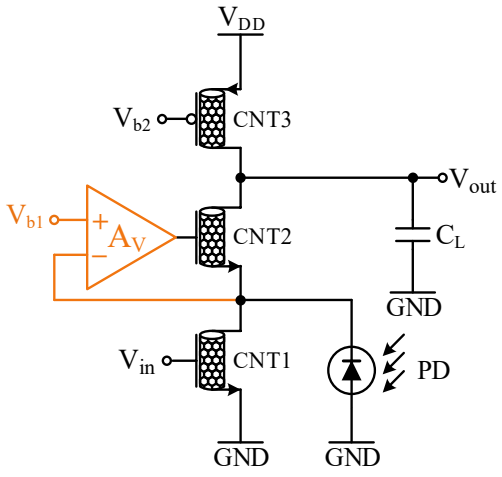


Figure 2. Conventional RGC-based TIA amplifier .

In the RGC topology, the gain-boosting effect can be represented as an increase in the effective transconductance of the driver transistor by a factor of $1+A_{v,CS}$, where $A_{v,CS}$ denotes the voltage gain of the CS stage. Accordingly, the midband input impedance of the structure can be written as :

$$Z_{in,RGC} = \frac{r_{ds2}}{1 + g_{m2}(1 + A_{v,CS})r_{ds2}} \quad (1)$$

As indicated by equation (1), the input impedance is reduced by approximately a factor of $1+A_{v,CS}$ relative to that of a conventional CG amplifier. Consequently, the effect of the input pole on bandwidth limitation is alleviated, allowing the dominant pole to move toward a higher frequency. Based on the small-signal analysis of a conventional RGC structure, the low-frequency transimpedance gain is expressed as :

$$Z_T = \frac{V_{out}}{I_{PD}} = \frac{g_{m2}r_{ds3}r_{ds2}r_{ds1}(1 + A_{v,CS}) + r_{ds3}r_{ds1}}{r_{ds3} + r_{ds2} + r_{ds1} + g_{m2}r_{ds2}r_{ds1}(1 + A_{v,CS})} \quad (2)$$

Despite these advantages, the conventional RGC topology is subject to headroom limitations in low-voltage designs. Specifically, the drain-source voltage of transistor CNT1 must remain sufficiently large to ensure that CNT4 can properly regulate the feedback path. Furthermore, if the input pole remains at a relatively low frequency, achieving the target bandwidth requires the use of bandwidth-extension techniques together with accurate output-pole compensation .

Proposed Transimpedance Amplifier

Figure 3 shows the proposed low-power TIA. The core circuit is implemented using a single-stage RGC topology composed of CNT1–CNT5. To improve bias controllability and stabilize the operating condition of the core devices, CNT7 is used as a pass transistor to adjust the control voltage applied to the gate of CNT4. In addition, CNT8 is configured as a diode-connected load, thereby introducing a small-signal resistance at the output node. By properly reducing this resistance, the output time constant is decreased, which moves the corresponding output pole toward higher frequencies and contributes to the extension of the −3 dB bandwidth. In accordance with the design targets of high bandwidth and low-power consumption, a single-stage transistor-only structure is adopted to reduce circuit complexity, decrease the occupied chip area, and facilitate circuit-level integration.

For analytical evaluation, the input photodiode is modeled by an equivalent current source, representing the photo-generated current, in parallel with a shunt capacitance associated with the depletion-region junction capacitance. This capacitance strongly affects the input frequency response; therefore, reducing its effective impact is essential for improving the high-frequency operation of the photodiode interface ,.

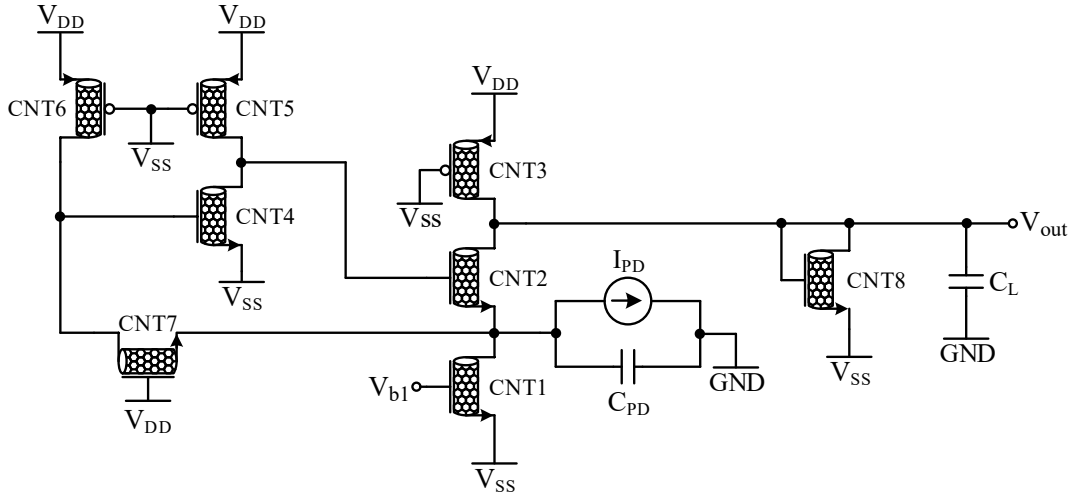


Figure 3. Proposed RGC-based TIA topology incorporating pass-transistor and diode-connected structures.

In the diode-connected structure illustrated in Figure 4(a), the gate and drain terminals are short-circuited. Under appropriate biasing conditions, this connection keeps the transistor in the saturation region and allows it to behave as an effective small-signal resistance. To determine the corresponding resistance, the low-frequency small-signal equivalent circuit shown in Figure 4(b) is considered. By applying a test voltage V_T, the equivalent input resistance R_{in} is obtained from the ratio V_T/I_T, as represented by the simplified model in Figure 4(c) .

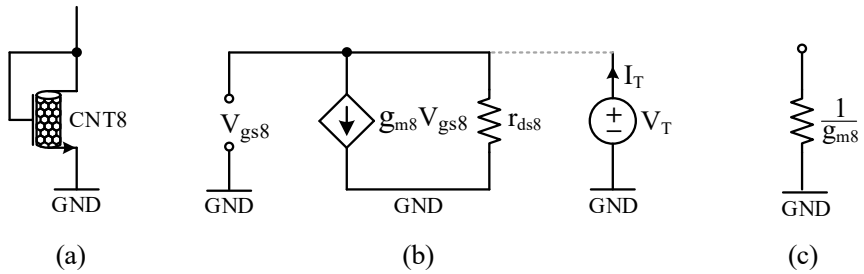


Figure 4. (a) Diode-connected transistor, (b) its small-signal equivalent model, and (c) the corresponding simplified small-signal equivalent model .

The test current I_T can be written as

$$i_T = \frac{v_T}{r_{ds8}} + g_{m8}v_{gs8} \xrightarrow{v_{gs8}=v_T} i_T = \frac{v_T}{r_{ds8}} + g_{m8}v_t = v_t\left(\frac{1}{r_{ds8}} \| g_{m8}\right) \tag{3}$$

Thus, the equivalent input resistance is obtained as

$$R_{in} = \frac{v_T}{i_T} = \left(r_{ds8} \| \frac{1}{g_{m8}}\right) \xrightarrow{r_{ds8} \gg 1/g_{m8}} R_{in} = \frac{1}{g_{m8}} \tag{4}$$

Accordingly, CNT8 provides a low effective resistance at the output node. Decreasing this resistance reduces the output time constant, shifts the output pole to a higher frequency, and consequently improves the bandwidth .

The small-signal equivalent circuit of the proposed RGC-based TIA is depicted in Figure 5.

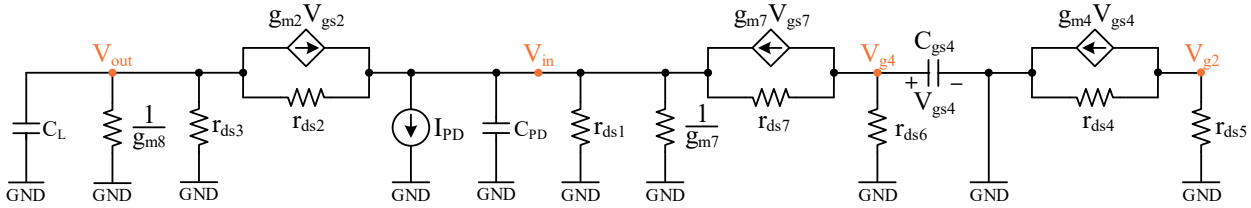


Figure 5. Small-signal equivalent circuit of the proposed RGC-based TIA.

Based on this model, is applied at the main circuit nodes. At the output node, the following relation is obtained:

$$\frac{V_{out}}{(1/g_{m8})} + \frac{V_{out}}{r_{ds3}} + g_{m2}V_{gs2} + \frac{V_{out} - V_{in}}{r_{ds2}} = 0 \tag{5}$$

At the input node, KCL gives

$$I_{PD} + \frac{V_{in}}{r_{ds1}} + \frac{V_{in}}{(1/g_{m7})} = g_{m2}V_{gs2} + \frac{V_{out} - V_{in}}{r_{ds2}} + g_{m7}V_{gs7} + \frac{V_{g4} - V_{in}}{r_{ds7}} \tag{6}$$

Similarly, the KCL equations at the gate node of CNT4 and the gate node of CNT2 are respectively expressed as

$$g_{m7}V_{gs7} + \frac{V_{g4} - V_{in}}{r_{ds7}} + \frac{V_{g4}}{r_{ds6}} = 0 \tag{7}$$

and

$$g_{m4}V_{gs4} + \frac{V_{g2}}{r_{ds4}} + \frac{V_{g2}}{r_{ds5}} = 0 \tag{8}$$

By solving these equations for V_{g2}, V_{g4}, and V_{in}, the transimpedance gain Z_T is derived as

$$Z_T = \frac{V_{out}}{I_{PD}} = \frac{1}{\left(-AD + g_{m2}ABC + \frac{1}{r_{ds2}} + \frac{AB}{r_{ds7}}\right)} \tag{9}$$

where the coefficients A, B, C, and D are defined as

$$A = \frac{V_{in}}{V_{out}} = \frac{\left(g_{m8} + \frac{1}{r_{ds3}} + \frac{1}{r_{ds2}}\right)}{\left(\frac{g_{m2}g_{m4}\left(g_{m7} + \frac{1}{r_{ds7}}\right)}{\left(\frac{1}{r_{ds4}} + \frac{1}{r_{ds5}}\right)\left(\frac{1}{r_{ds6}} + \frac{1}{r_{ds7}}\right)} + g_{m2} + \frac{1}{r_{ds2}}\right)} \tag{10}$$

$$B = \frac{V_{g4}}{V_{in}} = \frac{\left(g_{m7} + \frac{1}{r_{ds7}}\right)}{\left(\frac{1}{r_{ds6}} + \frac{1}{r_{ds7}}\right)} \tag{11}$$

$$C = \frac{V_{g2}}{V_{g4}} = \frac{-g_{m4}}{\left(\frac{1}{r_{ds4}} + \frac{1}{r_{ds5}}\right)} \tag{12}$$

$$D = g_{m2} + 2g_{m7} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds7}} \tag{13}$$

The frequency-domain analysis indicates that the proposed structure contains two principal poles. The input pole is given by

$$\omega_{p,in} = -\frac{1}{R_{in}C_{in}} \tag{14}$$

where R_{in} and C_{in} denote the equivalent resistance and capacitance at the input node, respectively:

$$R_{in} = r_{ds1} \left\| \frac{1}{g_{m7}} \right\| \frac{r_{ds6} + r_{ds7}}{1 + g_{m7}r_{ds7}} \left\| \frac{\left(\frac{1}{g_{m8}} \| r_{ds3}\right) + r_{ds2}}{1 + g_{m2}\left(1 + g_{m4}(r_{ds4} \| r_{ds5})\right)r_{ds2}} \right. \tag{15}$$

$$C_{in} = C_{PD} + C_{dg1} + C_{db1} + C_{sg2} + C_{sb2} + C_{sg7} + C_{sb7} \tag{16}$$

For the proposed circuit, the output pole is assumed to be dominant and is expressed as

$$\omega_{p,out} = -\frac{1}{R_{out}C_{out}} \tag{17}$$

where R_{out} and C_{out} are the equivalent resistance and capacitance at the output node, respectively:

$$R_{out} = \left[g_{m2}\left(1 + g_{m4}(r_{ds4} \| r_{ds5})\right)r_{ds2} \times \left(r_{ds1} \left\| \frac{1}{g_{m7}} \right\| \frac{r_{ds6} + r_{ds7}}{1 + g_{m7}r_{ds7}}\right)\right] \| r_{ds3} \| \frac{1}{g_{m8}} \approx r_{ds3} \| \frac{1}{g_{m8}} \tag{18}$$

$$C_{out} = C_L + C_{gs8} + C_{db8} + C_{dg3} + C_{db3} + C_{dg2} + C_{db2} \approx C_L \tag{19}$$

The low effective resistance introduced by CNT8, together with the dominant capacitive loading at the output node, provides the main mechanism for relocating the output pole to a higher frequency and enhancing the bandwidth of the proposed RGC topology.

To evaluate the noise sensitivity of the proposed circuit, the input-referred thermal noise of the RGC-based TIA is analyzed. According to the noise equivalent circuit shown in Figure 6, the dominant noise contributions originate from CNT2, CNT3, and CNT8 because these devices directly influence the signal-gain path and the output node. The input-referred noise current is defined as the ratio of the equivalent input noise voltage to the square of the TIA input impedance：

$$\overline{I_{n,in}^2} = \overline{V_{n,in}^2}/Z_{in}^2 \tag{20}$$

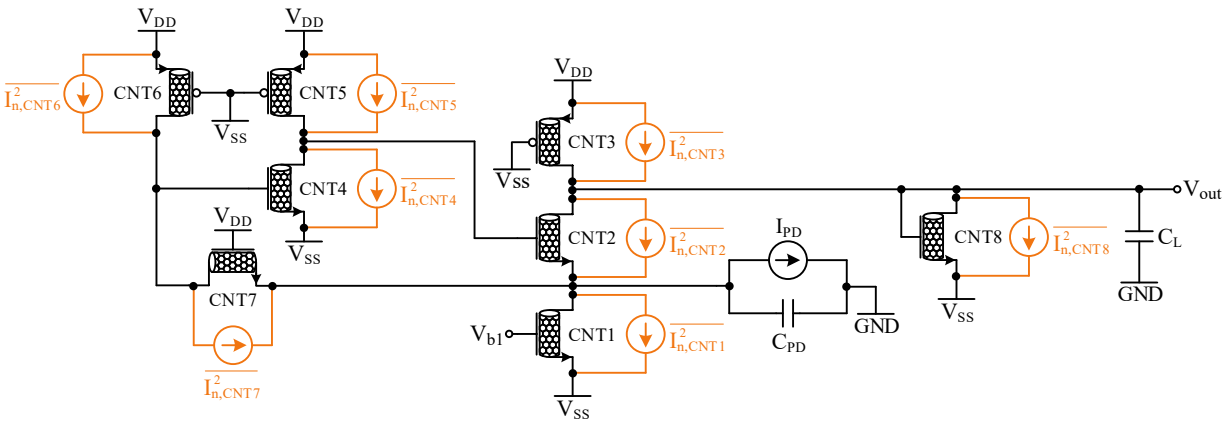


Figure 6. Noise equivalent circuit of the proposed RGC-based TIA.

The thermal noise currents generated by the transistors contributing to the output noise can be represented as the sum of independent noise components:

$$\overline{I_{n,out}^2} = \overline{I_{n,CNT2}^2} + \overline{I_{n,CNT3}^2} + \overline{I_{n,CNT8}^2} \tag{21}$$

Using the channel thermal-noise approximation, each noise component depends on the corresponding transconductance and thermal-noise factor:

$$\overline{I_{n,out.i}^2} = 4KT\gamma g_{m2} \tag{22}$$

Accordingly, the output thermal-noise voltage generated by the driver and load devices at the output node is obtained as

$$\overline{V_{n,out}^2} = \overline{I_{n,out}^2} \times |R_{out}|^2 = 4KT\gamma\left[g_{m2}\left(1 + g_{m4}(r_{ds4}\|r_{ds5})\right) + g_{m3} + g_{m8}\right] \times \left(r_{ds3}\|\frac{1}{g_{m8}}\right)^2 \tag{23}$$

To refer the output noise to the input, the voltage gain of the proposed RGC-based TIA is approximated as

$$|A_V| = \frac{V_{out}}{V_{in}} \approx g_{m2}\left(1 + g_{m4}(r_{ds4}\|r_{ds5})\right) \times \left(r_{ds3}\|\frac{1}{g_{m8}}\right) \tag{24}$$

Thus, for a voltage gain A_v, the input-referred noise voltage is given by :

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_v^2} = 4KT\gamma \frac{\left[g_{m2}\left(1 + g_{m4}(r_{ds4}\|r_{ds5})\right) + g_{m3} + g_{m8}\right]}{\left[g_{m2}\left(1 + g_{m4}(r_{ds4}\|r_{ds5})\right)\left(r_{ds3}\|\frac{1}{g_{m8}}\right)\right]^2} \tag{25}$$

Finally, the input-node referred noise current is calculated as

$$\overline{I_{n,in}^2} = \overline{V_{n,in}^2}/Z_{in}^2 = \overline{V_{n,in}^2}\Big/\left(R_{in}^2 + \frac{1}{C_{in}^2\omega^2}\right) \tag{26}$$

Equation (26) shows that reducing the input-referred noise requires not only the reduction of the effective noisy transconductance terms but also sufficient voltage gain and proper control of the input and output impedances. Therefore, by lowering the input impedance and shifting the output pole toward higher frequencies, the proposed RGC structure supports simultaneous improvement in high-bandwidth operation, transimpedance gain, and noise performance.

Simulation Results

The proposed TIA was evaluated using the Stanford CNTFET model. In all simulations, the supply voltage was set to ±0.45 V, while both the load capacitance C_L and photodiode capacitance C_{PD} were fixed at 10 fF. Following optimization of the CNTFET physical parameters, a chiral vector of (19,0) was selected, corresponding to a carbon-nanotube diameter of 1.5 nm and an approximate threshold voltage (V_{th}) of 0.28 V. The number of carbon nanotubes (N) was optimized to achieve a suitable trade-off between current-driving capability and power consumption, since increasing N quantizes the drain current and directly increases power dissipation. In addition, the nanotube pitch was fixed at the standard value of 20 nm to keep parasitic capacitances within a controllable range.

Table 1 summarizes the simulated performance of the proposed RGC-based TIA, and the corresponding frequency response is shown in Figure 7. By employing a diode-connected configuration, the proposed design achieves a transimpedance gain of 51.4 dBΩ, a −3 dB bandwidth of 28.3 GHz, an input-referred noise density of 5.3 pA/√Hz, and a power consumption of 368 μW, thereby satisfying the primary design targets.

Table 1. Simulation performance of the proposed RGC-based TIA.

	Z_T (dBΩ)	f_{-3dB} (GHz)	P_{diss} (μw)	IRN (pA/√Hz)	N1	N2	N3	N4	N5	N6	N7	N8
Required value	> 50	≈ 28	< 400	< 20	—	—	—	—	—	—	—	—
Simulation	51.4	28.3	368	5.3	20	40	35	1	2	1	2	30

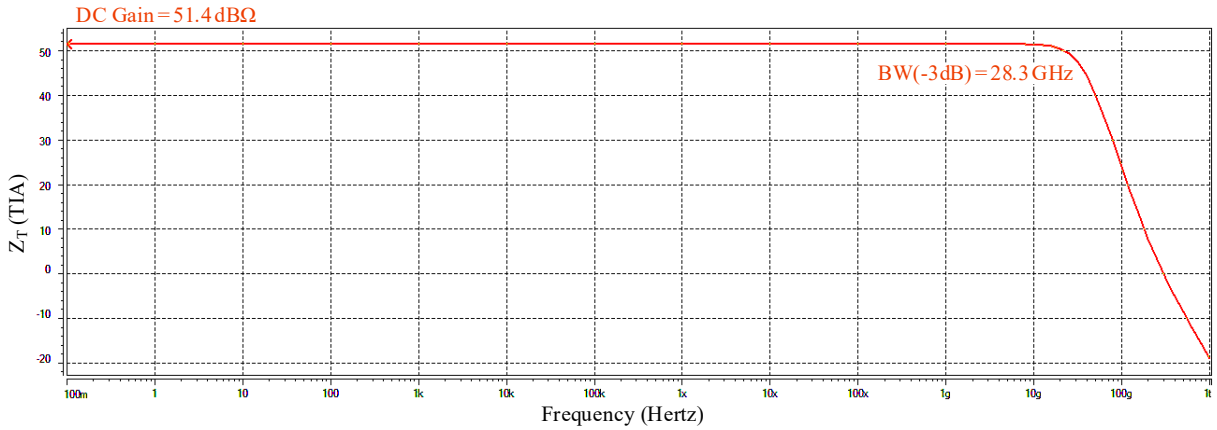


Figure 7. Simulated frequency response of the proposed RGC-based TIA topology.

The noise performance is illustrated in Figure 8. As observed in Figure 8(a), the input-referred noise density is 5.3 pA/√Hz at low frequencies and rises to 15.4 pA/√Hz at the −3 dB cutoff frequency. Furthermore, Figure 8(b) shows that the low-frequency output noise voltage density is expressed in 2 nV/√Hz.

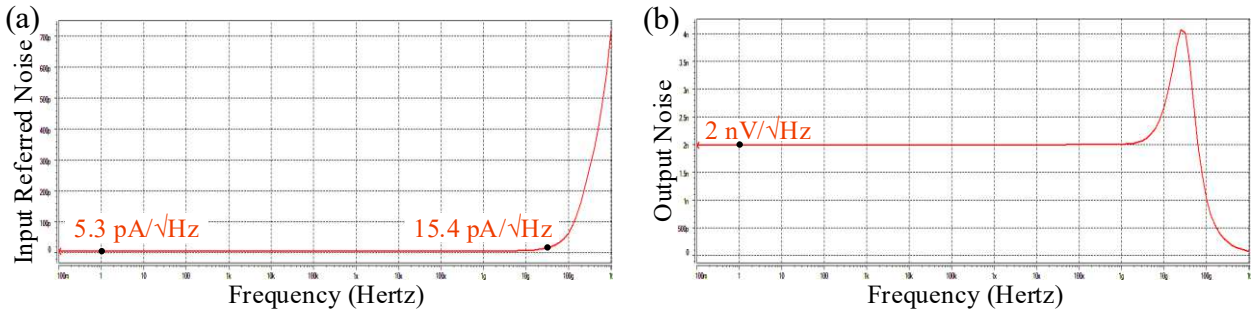


Figure 8. (a) Input-referred noise and (b) output noise of the proposed RGC-based TIA.

To assess output signal integrity, eye diagrams were simulated at 40 Gbps using a 2^7-1 non-return-to-zero (NRZ) pseudo-random binary sequence (PRBS) pattern. This analysis was carried out for input current amplitudes of 10 μA and 50 μA, with rise and fall times of 20 ps, as depicted in Figure 9. For the 10 μA input case, the vertical and horizontal eye openings are 3.05 mV and 24.36 ps,

respectively. When the input amplitude is increased to 50 μA, the corresponding eye openings become 15.02 mV and 23.89 ps. The clearly open eye diagrams in both cases confirm the proper operation of the proposed TIA at the target data rate.

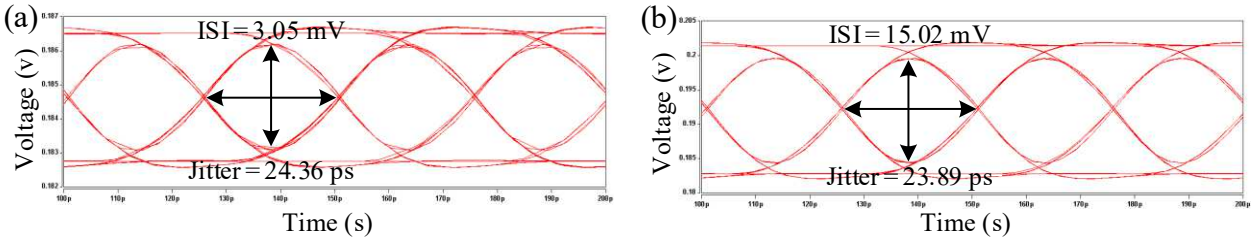


Figure 9. Simulated eye diagrams of the proposed RGC-based TIA for input current amplitudes of (a) 10 μA and (b) 50 μA.

To investigate sensitivity to process variations, Monte Carlo simulations were performed with emphasis on CNTFET threshold-voltage variations. As shown in Figure 10, a series voltage source was inserted at the gate of each transistor to emulate V_{th} variations. The nominal value of each source was set equal to the nominal threshold voltage of the corresponding transistor, and the variation was modeled using a Gaussian distribution with a standard deviation of ±10% over 200 simulation runs.

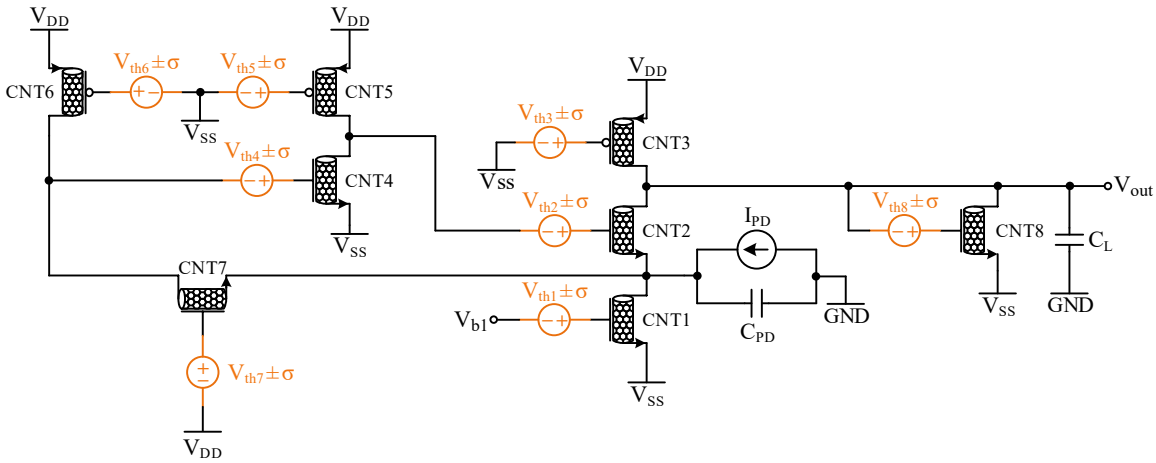


Figure 10. Proposed RGC-based TIA topology incorporating voltage sources for Monte Carlo modeling.

The resulting frequency responses, gain histogram, and bandwidth histogram are presented in Figure 11. Based on these distributions, the mean transimpedance gain is 60.5 dB and the mean bandwidth is 5.6 GHz. These results indicate that the circuit performance is sensitive to process-induced parameter variations.

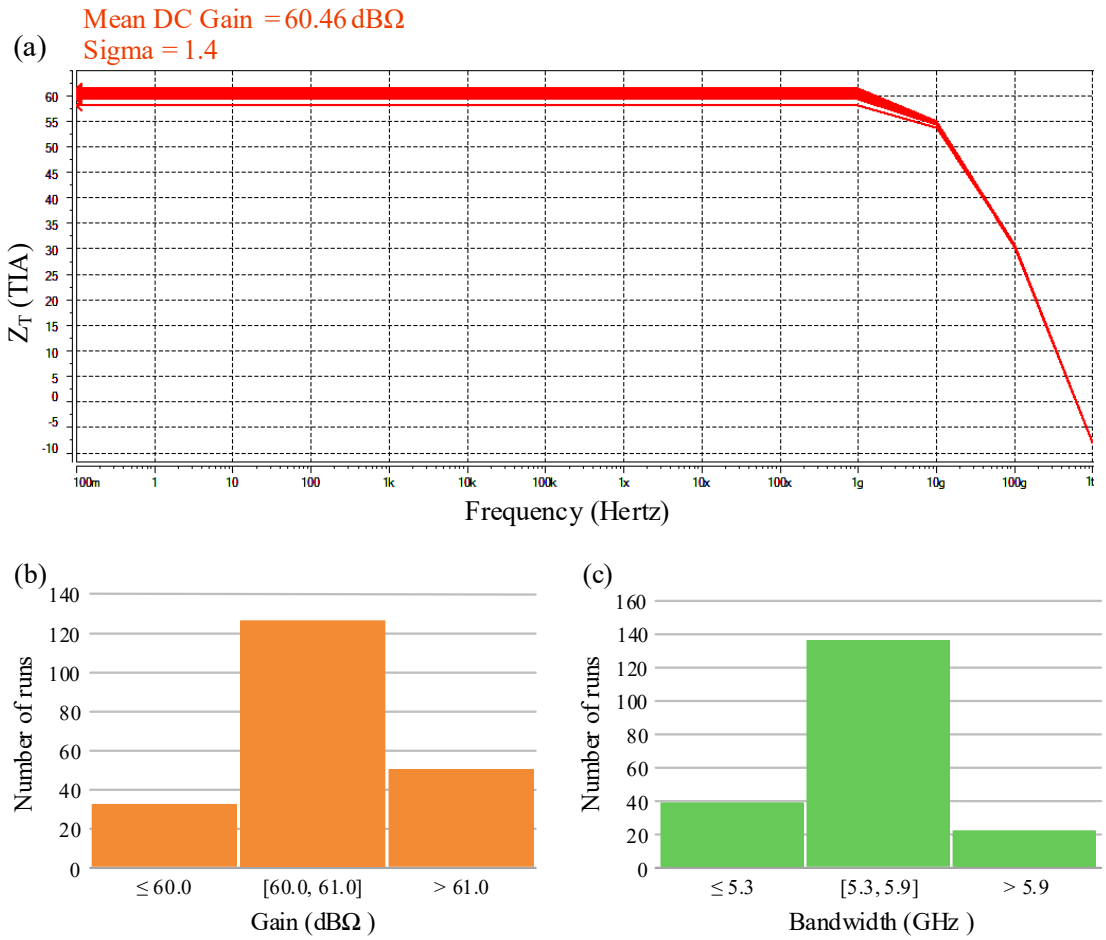


Figure 11. (a) Frequency response, (b) gain histogram, and (C) bandwidth histogram illustrating the effect of ±10% threshold-voltage variations on the frequency response of the proposed TIA topology.

The sensitivity of the TIA performance to supply voltage variation was also examined over the range from 0.4 V to 0.5 V. As summarized in Table 2, reducing the supply voltage slightly increases the transimpedance gain from 51.2 dBΩ to 51.6 dBΩ, whereas the bandwidth decreases from 28.8 GHz to 27.7 GHz. This modest reduction in bandwidth is attributed to degradation in transconductance, which shifts the dominant pole toward lower frequencies. Meanwhile, the power consumption decreases monotonically from 422 μW to 317 μW, whereas the input-referred noise remains nearly constant at approximately 5.3 pA/√Hz.

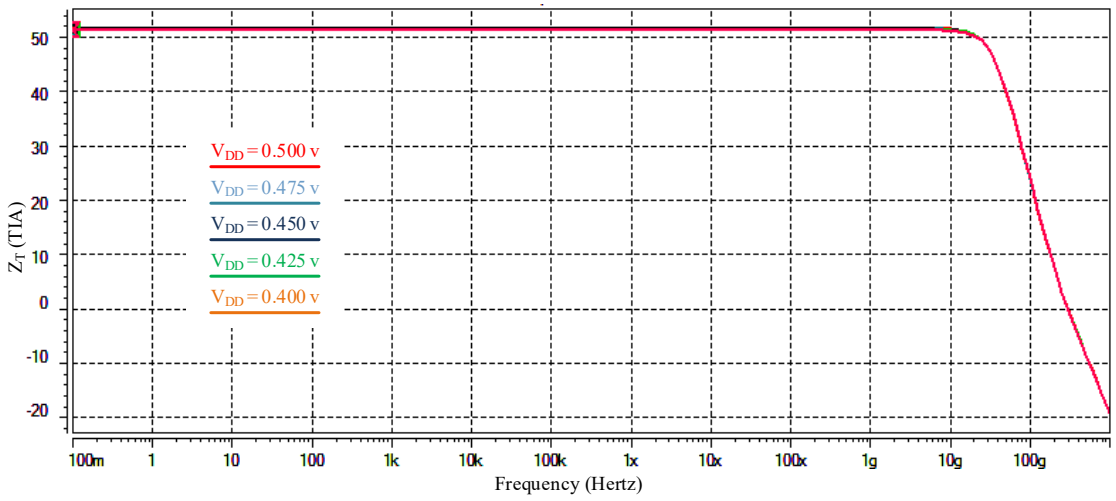


Figure 12. Sensitivity of the frequency response of the proposed TIA topology to supply voltage variations.

Overall, the combined use of the RGC-based TIA structure, gain-boosting mechanism, pass-transistor arrangement, and diode-connected configuration enables low-power consumption and strong tolerance to supply voltage variation while preserving the required gain and bandwidth.

Table 2. Simulated sensitivity of the proposed TIA performance to supply voltage variations.

V_{DD} (v)	Z_T (dBΩ)	BW (-3dB)	P_{diss}	IRN (A/√Hz)
0.500	51.2	28.8 GHz	422 µw	5.3 p
0.475	51.3	28.5 GHz	394 µw	5.3 p
0.450	51.4	28.3 GHz	368 µw	5.3 p
0.425	51.5	28.0 GHz	342 µw	5.3 p
0.400	51.6	27.7 GHz	317 µw	5.3 p

To benchmark the proposed design, its performance was compared with previously reported 40 Gbps optical receiver TIAs, as listed in Table 3. Two figures of merit (FOMs) were defined to evaluate the trade-offs among gain, bandwidth, power consumption, input-referred noise, and photodiode capacitance:

$$FOM1 = \frac{Gain\ (dB\Omega) \times Bandwidth\ (GHz)}{Power\ Consumption\ (mW) \times Input\ Referred\ Noise\ \left(pA/\sqrt{Hz}\right)} \quad (27)$$

$$FOM2 = \frac{Gain\ (dB\Omega) \times Bandwidth\ (GHz) \times C_{PD}\ (fF)}{Power\ Consumption\ (mW) \times Input\ Referred\ Noise\ \left(pA/\sqrt{Hz}\right)} \quad (28)$$

As indicated in Table 3, the proposed structure exhibits competitive performance in terms of transimpedance gain, bandwidth, power consumption, and noise. Simulated in 32-nm CNTFET technology, the proposed TIA achieves an FOM1 of 745.82 and an FOM2 of 7458.2. In comparison with the recent CNTFET-based designs in and , these values correspond to improvements of 56.5% and 16.6% in FOM1 and FOM2, respectively. This improvement is mainly attributable to the lower input-referred noise while maintaining competitive transimpedance gain and bandwidth. Therefore, the proposed circuit provides a favorable overall design trade-off relative to comparable CNTFET-based implementations.

Table 3. Comparison of the simulated performance of the proposed RGC-Based TIA with prior 40 Gbps designs.

	This work										
Year	2026	2026	2026	2022	2021	2015	2015	2012	2012	2010	2010
Process Technology	32nm CNTFET	32 nm CNTFET	32nm CNTFET	90nm MOSFET	0.18µm BiCMOS	0.13µm BiCMOS	65nm MOSFET	65nm MOSFET	45nm SOICMOS	65nm MOSFET	0.13µm MOSFET
Supply voltage	± 0.45 V	± 0.45 V	± 0.45 V	1 V	3.3 V	2.3 V	1.2 V	1.2 V	1 V	1.2 V	1.5 V
Data rate	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps
Gain	51.4 dBΩ	56.6 dBΩ	47.6 dBΩ	40 dBΩ	39.4 dBΩ	13 dB	50 dBΩ	54 dB	55 dBΩ	46.7 dBΩ	50 dBΩ
Bandwidth	28.3 GHz	28.0 GHz	28.4 GHz	25.8 GHz	32.9 GHz	43 GHz	33.1 GHz	25 GHz	30 GHz	21.6 GHz	29 GHz
Power consumption	368 µW	177 µW	183 µW	29 mW	77 mW	8.5 mW	–	–	9 mW	8.2 mW	45.7 mW
Input referred noise	5.3 pA/√Hz	14 pA/√Hz	15.5 pA/√Hz	25 pA/√Hz	37 pA/√Hz	–	–	–	20.47 pA/√Hz	30 pA/√Hz	51.8 pA/√Hz
C_{PD}	10 fF	10 fF	10 fF	–	–	17 fF	100 fF	60 fF	110 fF	200 fF	100 fF
C_L	10 fF	10 fF	10 fF	–	–	–	–	–	–	–	–
FOM1	745.82	639.54	476.58	1.42	0.4549	–	–	–	8.95	4.100	0.6125
FOM2	7458.2	6395.4	4765.8	–	–	–	–	–	985.18	820.09	61.25

Conclusion

In this work, an RGC-based transimpedance amplifier for 40-Gbps optical receivers was designed and simulated using 32 nm CNTFET technology. By combining an RGC core with low input resistance, a level-shifting pass transistor for proper biasing of CNT4, and a diode-connected load, the proposed structure enhances the frequency response of the circuit. The removal of resistors and inductors enables a fully transistor-based implementation and contributes to reduced chip area. At a supply voltage of ±0.45 V, the simulation results demonstrate a transimpedance gain of 51.4 dBΩ, a bandwidth of 28.3 GHz, a power consumption of 368 μW, and an input-referred noise of 5.3 pA/√Hz.

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Declaration

Competing interests

The authors declare no competing interests.

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