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***Abstract*—Multi-terminal high-voltage direct current (MT-HVDC) systems are increasingly used to enhance transmission flexibility and integrate offshore renewables. Due to the nonlinear power flow equations and multi-terminal couplings, the static voltage stability region (SVSR) of an MT-HVDC system is difficult to characterize. Existing numerical methods require extensive random sampling and repeated power-flow calculations for to achieve high accuracy, whereas approximation-based methods improve computational efficiency at the expense of conservative stability boundaries. This paper proposes a closed-loop active sampling method for SVSR characterization in MT-HVDC systems. First, a label-extension algorithm generalizes the solvability label of a verified terminal power profile to an expanded set, avoiding dense numerical simulations. A convex inner SVSR subset is constructed and represented explicitly in polyhedral form. Then, an iterative closed-loop procedure is developed to enlarge this subset by actively selecting the most informative terminal power profiles for numerical verification based on the current region geometry. The newly verified samples expand the SVSR subset and enable additional label extrapolation. Simulation case studies a representative MT-HVDC benchmark verify the validity of the proposed work.**

Keywords—Multi-terminal HVDC, static voltage stability region, active learning

I. INTRODUCTION

Multi-terminal high-voltage direct current (MT-HVDC) systems have been increasingly deployed to enhance transmission flexibility[1], facilitate offshore renewable integration[2], and interconnect asynchronous AC areas[3]. Compared with conventional point-to-point HVDC links, MT-HVDC systems exhibit stronger inter-terminal coupling and more intricate interactions among converter control loops, thereby posing greater challenges to system design and stable operation[1][4].

During operation, MT-HVDC systems are subject to continually varying terminal power profiles and operating points due to renewable fluctuations, market re-dispatch, and remedial control actions[5]. These variations continuously alter power-sharing patterns and redistribute voltage-support responsibilities among converter stations, thereby imposing stringent requirements on coordinated steady-state voltage regulation across the network.

Owing to the electrical coupling among terminals and the interactions among converter control loops, a change in the power injection at one terminal may affect voltage profiles and power balance throughout the entire MT-HVDC system. Under stressed operating conditions or following severe disturbances, inadequate or delayed voltage support from converter stations and associated control equipment may lead to pronounced voltage deviations that spread through the network. As the system approaches its operating limits, such deviations can progressively erode the existence margin of feasible steady-state equilibria and, in extreme cases, drive the system to the boundary of power-flow solvability, ultimately resulting in system-wide voltage collapse[6].

Therefore, it is essential to rapidly assess whether a candidate terminal power profile admits a feasible steady-state operating point. This motivates the characterization of the static voltage stability region (SVSR), defined as the set of terminal power profiles for which the MT-HVDC system possesses at least one steady-state equilibrium satisfying the corresponding power-flow equations.

Accurate SVSR characterization is crucial for secure scheduling, fast corrective control, and risk-aware early warning in MT-HVDC systems. However, obtaining the SVSR analytically is challenging because the steady-state power-flow equations of MT-HVDC systems are nonlinear, and the SVSR boundary is implicitly determined by the coupled relationship between terminal power injections and steady-state voltages[7][8]. Consequently, the boundary generally does not admit a closed-form representation[9][10], and its accurate identification requires extensive sampling over the entire terminal-power-profile space together with repeated nonlinear power-flow solvability tests..

To obtain an accurate SVSR boundary, numerical methods have been developed that randomly sample a large number of terminal power profiles to generate representative operating scenarios that capture SVSR geometry, and then determine the security or stability label of each sample via iterative simulation or steady-state evaluation[10][11][12]. For example, Ref. [10] proposed a relaxed decoupled direct calculation method for voltage collapse points and integrated it with boundary tracking to form the SVSR boundary. Ref. [12] developed a time-series data-driven framework for batch voltage-security assessment by constructing and labeling a large number of operating cases through simulation. Iterative steady-state solvers are executed to determine its SVSR containment label. As a result, directly characterizing the SVSR through exhaustive numerical testing becomes computationally burdensome, particularly when the number of terminals and the uncertainty dimension increase.

To reduce computational burden, approximation methods have been developed to replace the implicit SVSR boundary with tractable surrogates, thereby enabling fast online screening[13][14][15]. For instance, Ref. [13] derived an explicit linear approximation to the nonlinear power-flow solution together with error bounds, providing a computationally efficient surrogate for feasibility assessment in power-injection space. In addition, Ref. [14] proposed a global parametric polynomial approximation of SVSR boundaries, which enables direct boundary representation without exhaustive pointwise computation. Ref. [15] studied practical steady-state security-region boundary characterization in distribution grids and further improved the identification of critical boundary hyperplanes for accurate region approximation. Nevertheless, the improved tractability is often achieved at the expense of boundary fidelity, especially near critical operating conditions, which may underestimate admissible operating ranges and weaken decision support for preventive scheduling and corrective actions.

Moreover, most existing stability studies on MT-HVDC systems have been conducted within a dynamic-stability framework, with primary emphasis on small-signal interaction modes, impedance analysis, and large-signal disturbance behavior[16][17][18][19][20]. For example, Ref. [18] investigated the identification and analysis of interaction modes in MT-HVDC systems from a small-signal perspective, revealing how converter dynamics and control parameters shape modal interactions. Ref. [20] studied the large-signal stability of MT-HVDC systems based on mixed potential theory, providing insights into nonlinear stability under severe disturbances. However, SVSR characterization has received limited attention in the MT-HVDC literature. There is a pressing need for fast and accurate SVSR characterization methods for MT-HVDC systems.

To address these issues, we propose a closed-loop active sampling method to characterize the SVSR in MT-HVDC systems. The approach reduces computational workload through sample filtering and label extrapolation. First, we develop a label-extension algorithm that transfers the SVSR-containment label from a verified terminal power profile to an expanded set of profiles, avoiding dense random simulations in existing numerical methods. Then, we construct a convex SVSR subset from the expanded sets and represent it in an explicit polyhedral form. The subset is enlarged via an iterative closed-loop procedure. In each iteration, we actively select a small batch of new power profiles for numerical verification. The updated region geometry is used to recommend the most informative candidates in subsequent iterations. The newly verified samples further enlarge the SVSR subset and enable additional label extrapolation.

Our main contributions are three-fold.

1) We establish a steady-state equivalent model for MT-HVDC systems in the terminal-power-profile parameter space. The model captures the steady-state power-flow relationship between terminal power injections and dc network voltages, and provides the analytical foundation for characterizing the SVSR of MT-HVDC systems.

2) We propose a network-informed framework for SVSR characterization in MT-HVDC systems. The framework combines steady-state solvability testing with label extrapolation to construct a guaranteed inner SVSR subset from a limited number of verified terminal power profiles, which reduces the need for large-scale random sampling, thereby reducing the need for large-scale random sampling. Furthermore, we develop an iterative inner-approximation refinement scheme that expands the obtained SVSR subset, progressively tightening the SVSR characterization with reduced conservativeness.

3) We design a closed-loop active sampling strategy for efficient SVSR refinement. The proposed strategy selects informative terminal power profiles for numerical verification according to the geometry of the current SVSR approximation, so that computational effort is concentrated on the most impactful candidates. As a result, the proposed method further improves the efficiency of SVSR characterization.

The remainder of this paper is organized as follows. Section II presents the steady-state equivalent formulation of the MT-HVDC system, and casts SVSR characterization as a region-identification problem in the terminal power-profile space and defines the corresponding static voltage stability region. Section III develops the proposed closed-loop active sampling method, comprising network-informed label extrapolation, inner-region refinement, and sample recommendation. Section IV provides numerical studies on representative MT-HVDC systems to validate the accuracy and computational efficiency of the proposed approach. Section V concludes the paper and outlines future research directions.

II. System Modeling

In this paper, an MT-HVDC system based on voltage source converters (VSCs) is adopted for modeling and analysis. An example of the three-terminal HVDC system topology is illustrated in Fig. 1. It consists of one sending-end AC grid source, two receiving-end loads, and the dc transmission cables interconnecting the three terminals. In the following, the source, the dc transmission cables, and the loads are modeled separately.

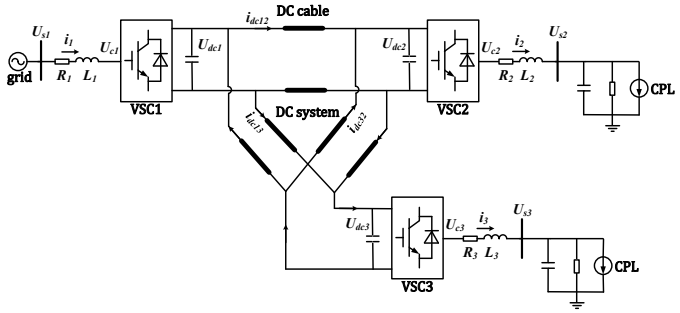


Fig. 1. Topology of the Example Three-Terminal HVDC System

A. Steady-State Model

1) Source-side modeling: We first establish the model of the source-side terminal. The control structure of the rectifier-side converter, denoted as VSC1, is shown in Fig. 2. As can be seen, the rectifier is responsible for regulating the DC-side voltage[21]. Specifically, active power control is realized by regulating the DC voltage U_{dc1} to its reference value U_{dcr} through the cascaded outer-loop and inner-loop controllers on the d-axis, while reactive power control is achieved by driving the reactive current i_{1q} to zero through the q-axis inner-loop controller. Here, k_{p1} and k_{i1} denote the proportional and integral gains of the voltage-loop PI controller, respectively, whereas k_{p2}, k_{p3}, k_{i2}, and k_{i3} represent the proportional and integral gains of the current-loop PI controllers. The state variables x_1, x_2, and x_3 correspond to the integrator states of the PI controllers.

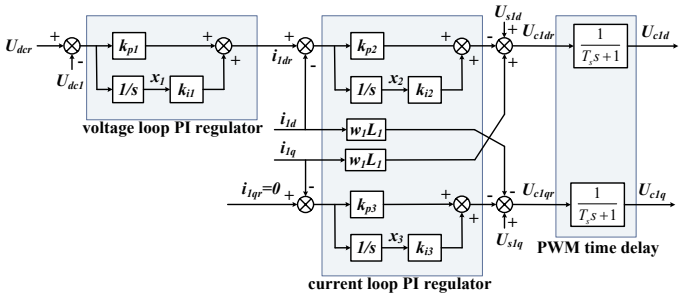


Fig. 2. DC voltage control structure of the AC/DC rectifier.

It is worth noting that the sending-end converter typically regulates U_{dc1} to a prescribed reference value through the aforementioned control scheme. Therefore, from the steady-state perspective adopted in this paper, the source-side terminal can be equivalently represented as a controlled voltage source.

2) DC cable modeling: The DC transmission cable is represented by a π-equivalent impedance model, as shown in Fig. 3. Here, L_{cab}, R_{cab}, and C_{cab} denote the lumped equivalent inductance, resistance, and capacitance of the cable, respectively. These equivalent parameters scale proportionally with the cable length and are used to capture the dominant electrical characteristics of the DC transmission line.

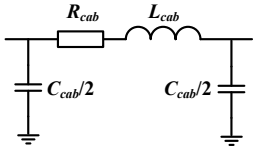


Fig. 3. π-Equivalent Impedance Model of the DC Transmission Cable.

3) Load-side modeling: In the steady-state MT-HVDC model, both active and passive receiving-end terminals can be equivalently represented as constant power loads (CPLs) when viewed from the DC side. The active receiving-end terminal operates under constant-power control and directly regulates its DC-side power exchange, while the passive receiving-end terminal adopts constant-AC-voltage control and draws DC-side input power determined by the supplied load demand. Therefore, both inverter-side terminals exhibit CPL characteristics in the DC network. The corresponding negative incremental impedance model is illustrated in Fig. 4.

The power characteristic of the CPL is given by

$$ui = p_{\text{const}}, \tag{1}$$

where p_{const}, u, and i denote the load power, input voltage, and input current, respectively.

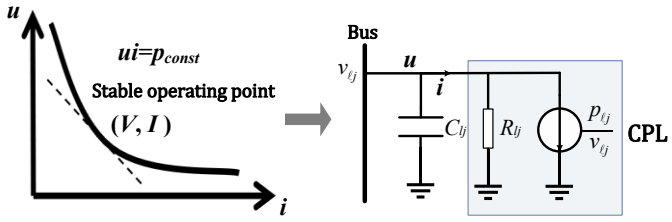


Fig. 4. Negative Incremental Impedance Model of a Constant Power Load.

By performing a first-order Taylor expansion of the above relation around a steady-state operating point (V, I), where V and P_{const} denote the steady-state voltage and power, respectively, the load current can be approximated as

$$i \approx 2\frac{P_{\text{const}}}{V} - \frac{P_{\text{const}}}{V^2}u. \tag{2}$$

Accordingly, the CPL can be represented by an equivalent current source I_i in parallel with a small-signal impedance R_i, where

$$\begin{cases} R_i = -\dfrac{V^2}{P_{\text{const}}}, \\ I_i = 2\dfrac{P_{\text{const}}}{V}. \end{cases} \tag{3}$$

It can be seen from (3) that R_i is negative, which indicates the negative incremental impedance characteristic of the CPL. This property plays a critical role in shaping the static voltage stability characteristics of the HVDC system and is explicitly taken into account in the subsequent SVSR analysis.

4) Overall steady-state model: Based on the source-side, DC-cable, and load-side models established above, the MT-HVDC system can be represented in steady state by an equivalent DC network. For the static analysis considered in this paper, the AC-side steady-state effects are absorbed into equivalent terminal representations. Specifically, the sending-end converter is represented as a controlled voltage source, while the receiving-end converters are represented as constant power loads. Based on these equivalent steady-state representations, the existence and feasibility of system operating points are determined by the equilibrium conditions of the interconnected DC network formed by the terminal nodes and DC transmission cables.

Therefore, the static voltage stability property of the MT-HVDC system can be analyzed through the solvability of an equivalent DC network model. For the illustrative three-terminal HVDC system considered in this paper, the resulting equivalent static DC network is shown in Fig. 5, where one node represents the source terminal and the other two nodes represent load terminals. The steady-state model of the MT-HVDC system can be equivalently cast as a DC network model. This equivalent representation serves as the analytical basis for recasting MT-HVDC static security assessment as an SVSR characterization problem in the terminal-power-profile space. The corresponding formulation is presented in the next subsection.

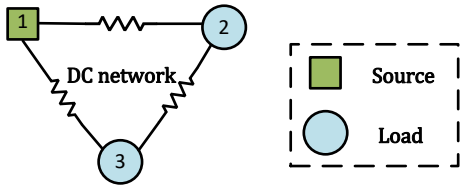


Fig. 5. Equivalent DC Network Representation of the Illustrative Three-Terminal MT-HVDC System.

B. Power-Flow Analysis

In the steady-state representation developed in Section II-A, the sending-end source model is treated as a source node, each receiving-end converter represented by a CPL is treated as a load node, and each DC cable model is treated as a transmission line interconnecting the corresponding terminal nodes. With these correspondences, the MT-HVDC system can be recast as a DC power-flow network for static security analysis.

Building on the steady-state equivalent representation established in Section II-A, we consider a DC network comprising n_l load nodes and n_s source nodes. If node k is connected to node j, we denote this relation by $k \sim j$; otherwise, $k \nsim j$. Let $w_{kj} = w_{jk} > 0$ denote the conductance of the transmission line connecting nodes k and j. The network topology and line conductances are described by the weighted Kirchhoff matrix $Y \in \mathbb{R}^{(n_l+n_s)\times(n_l+n_s)}$, defined as

$$Y_{kj} \triangleq \begin{cases} \sum_{i\sim k} w_{ki}, & k = j, \\ -w_{kj}, & k \neq j,\ k \sim j, \\ 0, & k \neq j,\ k \nsim j. \end{cases} \tag{4}$$

We further partition Y according to whether a node is a load node or a source node, i.e.,

$$Y = \begin{bmatrix} Y_{ll} & Y_{ls} \\ Y_{sl} & Y_{ss} \end{bmatrix}. \tag{5}$$

Under standard connectivity assumptions, Y_{ll} and Y_{ss} are symmetric positive definite principal submatrices of Y.

Let $p_l = [p_{l1}, \dots, p_{ln_l}]^\top \in \mathbb{R}^{n_l}$ denote the vector of constant-power demands at the load nodes, where each component corresponds to the DC-side power absorbed by a receiving-end converter represented as a CPL in Section II-A. Let $v_l = [v_{l1}, \dots, v_{ln_l}]^\top \in \mathbb{R}^{n_l}$ denote the corresponding vector of load-node voltages. Similarly, let $v_s = [v_{s1}, \dots, v_{sn_s}]^\top \in \mathbb{R}^{n_s}$ denote the vector of source-node voltages, and let $V^{\mathrm{ref}} = [V_1^{\mathrm{ref}}, \dots, V_{n_s}^{\mathrm{ref}}]^\top \in \mathbb{R}^{n_s}$ denote the vector of prescribed source-voltage setpoints. Please recall that each entry of V^{ref} corresponds to the regulated DC terminal voltage of a source-side converter, such as U_{dc1} in the three-terminal example introduced in Fig.2. Therefore, the vectors p_l and V^{ref} provide the power-demand and voltage-control parameterization, respectively, of the MT-HVDC steady-state model in the terminal-power-profile space.

Let $V = \begin{bmatrix} v_l \\ v_s \end{bmatrix} \in \mathbb{R}^{n_l+n_s}$ denote the network voltage vector, where all node voltages are assumed to be positive, i.e., $V > 0$. Let $I \in \mathbb{R}^{n_l+n_s}$ denote the vector of currents injected into the network. The nodal power injection vector is then given by

$$p = \mathrm{diag}(V)\, I \in \mathbb{R}^{n_l+n_s}, \tag{6}$$

where $p < 0$ corresponds to power consumption at load nodes, whereas $p > 0$ corresponds to power injection from source nodes.

By Kirchhoff's and Ohm's laws, the nodal power injections satisfy

$$\begin{bmatrix} p_l \\ p_s \end{bmatrix} = \mathrm{diag}\left(\begin{bmatrix} v_l \\ v_s \end{bmatrix}\right) \begin{bmatrix} Y_{ll} & Y_{ls} \\ Y_{sl} & Y_{ss} \end{bmatrix} \begin{bmatrix} v_l \\ v_s \end{bmatrix}. \tag{7}$$

Let v_l^e denote the steady-state voltage vector at the load nodes, and let p_s denote the source-node power injection vector. Since the source nodes are regulated to track the prescribed voltage references V^{ref}, the steady-state operating point of the MT-HVDC system satisfies

$$\begin{cases} p_s = \mathrm{diag}(V^{\mathrm{ref}})\left(Y_{sl}v_l^e + Y_{ss}V^{\mathrm{ref}}\right), \\ p_l = \mathrm{diag}(v_l^e)\left(Y_{ll}v_l^e + Y_{ls}V^{\mathrm{ref}}\right). \end{cases} \tag{8}$$

Here, Y_{ss}, Y_{sl}, and Y_{ll} represent the source-source, source-load, and load-load subnetworks, respectively, with $Y_{sl} = Y_{ls}^{\top}$, $Y_{ss} \in \mathbb{R}^{n_s \times n_s}$, $Y_{ls} \in \mathbb{R}^{n_l \times n_s}$, and $Y_{ll} \in \mathbb{R}^{n_l \times n_l}$. It can be observed from the second relation in (8) that, for a given load-power profile p_l, the power-flow equation is quadratic in the steady-state voltage v_l^e. Consequently, under sufficiently stressed loading conditions, the power-flow equations may fail to admit a real positive solution.

In general, a solution to the power-flow equations in (8) corresponds to a steady-state equilibrium of the MT-HVDC system. Therefore, loss of power-flow solvability may indicate the onset of static voltage instability. Therefore, accurately characterizing the set of terminal power profiles for which (8) remains solvable is of fundamental importance for static security assessment. This observation motivates the SVSR analysis developed in the subsequent section.

C. SVSR Characterization Problem

Although the source-side terminals of the MT-HVDC system are regulated to prescribed DC-voltage setpoints, the steady-state operating condition of the overall system is not fixed. In practice, the receiving-end terminal powers vary continuously due to renewable generation fluctuations, dispatch adjustments, and operating-condition changes in the interconnected network. In the steady-state equivalent model established above, such variations are reflected as changes in the terminal power profile, which in turn reshape the equilibrium DC-voltage distribution of the MT-HVDC system. When the operating condition becomes sufficiently stressed, the steady-state equations may cease to admit a feasible solution, indicating loss of static voltage security.

For the MT-HVDC system considered in this paper, the source-side terminals are modeled as voltage-controlled nodes with prescribed setpoints V^{ref}, whereas the receiving-end terminals are modeled as constant-power nodes. Accordingly, the static security of the MT-HVDC system can be assessed through the solvability of the steady-state network equations in (8). This motivates the definition of the static voltage stability region (SVSR) in the terminal-power-profile space.

Definition 1: For a given source-voltage setpoint vector V^{ref}, the SVSR of the MT-HVDC system is defined as the set of load-side terminal power profiles p_l for which there exists at least one admissible steady-state voltage solution v_l^e satisfying the MT-HVDC power-flow equations, i.e.,

$$\mathcal{P}_l := \{p_l \in \mathbb{R}^{n_l} \mid \exists\, v_l^e > 0 \text{ s.t. (8) is solvable}\}. \tag{9}$$

Equivalently, if one defines the terminal power injection vector $p = [p_l^{\top}, p_s^{\top}]^{\top}$ and the steady-state voltage vector $v = [(v_l^e)^{\top}, (V^{\mathrm{ref}})^{\top}]^{\top}$, the admissible operating region of the MT-HVDC system can be interpreted as the set of terminal power profiles for which the steady-state network equations admit at least one equilibrium. Under the source-voltage-controlled formulation adopted in this paper, this characterization reduces to the region $\mathcal{P}_l$ in the receiving-end terminal-power space.

The region $\mathcal{P}_l$ provides a direct description of the statically secure operating range of the MT-HVDC system. Any point inside $\mathcal{P}_l$ corresponds to a terminal power profile for which the MT-HVDC system possesses at least one feasible steady-state operating point, whereas operating conditions outside $\mathcal{P}_l$ are associated with loss of steady-state solvability. Therefore, accurate characterization of $\mathcal{P}_l$ is essential for static security assessment of MT-HVDC systems.

However, explicit characterization of $\mathcal{P}_l$ is challenging. The SVSR boundary is specified implicitly by the nonlinear steady-state equations of the MT-HVDC system and therefore generally lacks a closed-form expression. Consequently, existing numerical methods must rely on repeated solvability testing over many sampled terminal power profiles, leading to substantial computational cost. This difficulty is further aggravated as the number of terminals increases, since the terminal-power-profile space becomes higher-dimensional and exhaustive numerical exploration rapidly becomes intractable. Although approximation-based methods can reduce this burden by introducing prescribed surrogate regions or simplified boundary representations, they often yield conservative characterizations and limited fidelity near the true SVSR boundary.

Therefore, the problem considered in this paper is to efficiently characterize the region $\mathcal{P}_l$ in the receiving-end terminal-power space for a MT-HVDC system.

III. Proposed Approach

As discussed in Section II, static security assessment of an MT-HVDC system can be recast as the characterization of the region $\mathcal{P}_l$ in the receiving-end terminal-power space. A direct treatment of this problem would require repeated solvability checks of the nonlinear MT-HVDC steady-state equations for a large number of candidate terminal power profiles, which becomes computationally expensive as the number of terminals increases. To address this difficulty, this section develops a closed-loop active sampling method for SVSR characterization of MT-HVDC systems.

The proposed framework consists of two modules. The first module performs rapid feasibility labeling by constructing theoretically guaranteed inner subsets of the MT-HVDC SVSR from verified solvable terminal power profiles. Specifically, two types of guaranteed subsets are exploited: interval-based subsets, which are induced by individual verified profiles through monotone solvability, and a convex subset, which is induced by the collective geometry of multiple verified profiles through convexity. These subsets enable many candidate terminal power profiles to be labeled as solvable without additional numerical solution of the MT-HVDC power-flow equations. The second module performs closed-loop active sampling, where unlabeled terminal power profiles are selected according to the geometry of the current SVSR approximation and then numerically verified to further expand the guaranteed region. In this way, the proposed framework reduces the need for exhaustive pointwise

evaluation while progressively improving the fidelity of SVSR characterization for MT-HVDC systems.

A. Rapid Labeling via Interval-Based and Convex Subsets

The main computational bottleneck in MT-HVDC SVSR characterization lies in the repeated feasibility evaluation of candidate terminal power profiles. To reduce the number of numerical solvability checks, this subsection develops a rapid labeling mechanism that identifies a subset of candidate profiles as guaranteed solvable based on the geometric properties of the SVSR associated with the equivalent MT-HVDC DC network introduced in Section II.

Le $\mathcal{V} = \left\{p_l^{(i)}\right\}_{i=1}^{m} \subseteq \mathcal{P}_l$ denote the set of terminal power profiles that have already been verified to admit feasible steady-state operating points of the MT-HVDC system. Starting from this initial set, we construct two classes of guaranteed subsets in the receiving-end terminal-power space.

First, for each verified solvable profile $p_l^{(i)}$, an interval-based subset is induced according to the monotone solvability structure of the MT-HVDC steady-state model[22]. Specifically, if a candidate profile p_l satisfies $p_l \succeq p_l^{(i)}$, then p_l also admits at least one feasible steady-state operating point and therefore belongs to the SVSR. Therefore, the associated interval-based subset is defined as

$$\mathcal{S}_i^{\mathrm{int}} := \left\{p_l \in \mathbb{R}^{n_l} \mid p_l \succeq p_l^{(i)}\right\}, i = 1, \ldots, m, \tag{10}$$

where each $\mathcal{S}_i^{\mathrm{int}}$ is a guaranteed inner subset of the SVSR, and the union of all such subsets is given by $\mathcal{S}^{\mathrm{int}} := \bigcup_{i=1}^{m} \mathcal{S}_i^{\mathrm{int}}$.

Second, the SVSR geometry of the MT-HVDC system also admits a convex subset induced jointly by multiple verified solvable profiles[23]. Specifically, the convex subset generated by $\mathcal{V}$ is defined as

$$\mathcal{S}^{\mathrm{cvx}} := \mathrm{conv}(\mathcal{V}), \tag{11}$$

where $\mathrm{conv}(\cdot)$ denotes the convex hull operator.

The two subset constructions play complementary roles. The interval-based subsets provide low-cost extrapolation from each individual verified solvable profile and are particularly effective in extending the guaranteed region along monotone directions. The convex subset leverages the collective geometry of multiple verified profiles and enriches the inner approximation in regions where feasible operating points are correlated across dimensions. Combining the two yields a more informative guaranteed SVSR approximation than either construction alone.

Define the aggregate guaranteed subset as

$$\mathcal{S}^{\mathrm{g}} := \mathcal{S}^{\mathrm{int}} \cup \mathcal{S}^{\mathrm{cvx}}. \tag{12}$$

Let $\mathcal{V} \subseteq \mathcal{P}_l$ be a set of verified solvable terminal power profiles for the MT-HVDC system. Then the aggregate subset $\mathcal{S}^{\mathrm{g}}$ satisfies $\mathcal{S}^{\mathrm{g}} \subseteq \mathcal{P}_l$.

Based on this information, a candidate terminal power profile $\tilde{p}_l$ can be labeled without solving the MT-HVDC steady-state equations whenever it lies inside the guaranteed subset. Accordingly, the rapid feasibility-labeling rule is defined as

$$\ell(\tilde{p}_l) = \begin{cases} 1, & \tilde{p}_l \in \mathcal{S}^{\mathrm{g}}, \\ \text{undecided}, & \tilde{p}_l \notin \mathcal{S}^{\mathrm{g}}, \end{cases} \tag{13}$$

where $\ell(\tilde{p}_l) = 1$ indicates that $\tilde{p}_l$ is certified as solvable for the MT-HVDC system, and "undecided" means that no guaranteed conclusion is drawn at this stage.

This labeling mechanism serves as the first layer of the proposed framework. It enables a large portion of candidate terminal power profiles to be screened out as guaranteed feasible at negligible cost, thereby avoiding unnecessary repeated numerical evaluation of the MT-HVDC steady-state model. The remaining undecided profiles are then passed to the closed-loop active sampling module in Section III-B for targeted numerical verification and further SVSR refinement.

B. Geometry-Guided Closed-Loop Active Sampling

While Section III-A provides a guaranteed inner approximation of the MT-HVDC SVSR through interval-based subsets and a convex subset, the resulting region does not fully recover the true SVSR boundary. A considerable portion of the terminal-power-profile space therefore remains unlabeled. Since different unlabeled profiles contribute unequally to SVSR refinement, it is inefficient to continue numerical verification through random exploration. Instead, the refinement process should focus on those candidates that are most informative with respect to the current region estimate.

To this end, we develop a closed-loop active sampling strategy for MT-HVDC SVSR refinement. At each iteration, a classifier is used to estimate the posterior probability that a candidate terminal power profile belongs to the solvable region. Based on this probability, the uncertainty of each candidate profile p_l is quantified as

$$\mathcal{M}(p_l) = 1 - \left| 2F(p_l; \theta) - 1 \right|, \tag{14}$$

where $F(p_l; \theta) \in [0,1]$ denotes the posterior probability predicted by the current classifier. A larger value of $\mathcal{M}(p_l)$ indicates that the sample lies closer to the current decision boundary and is therefore more informative for SVSR refinement. Accordingly, the proposed method preferentially selects high-uncertainty terminal power profiles for numerical verification, appends the newly verified solvable samples to the existing set, and then reconstructs the interval-based subsets and convex subset in the next iteration. In this way, the SVSR characterization process is performed in a closed loop: the current region estimation guides subsequent sample acquisition, and the newly acquired labels further improve the region estimation.

The proposed framework constructs a guaranteed inner approximation of the MT-HVDC SVSR from numerically verified solvable terminal power profiles. Specifically, some verified profiles induce interval-based subsets through the monotone solvability property, while the entire set of verified

solvable profiles is further used to form a convex subset through convex-hull expansion. The union of these subsets defines the current guaranteed region. This mechanism allows the proposed method to enlarge the certified SVSR approximation in a structured manner, rather than relying solely on pointwise numerical labeling. Nevertheless, the guaranteed region does not fully recover the true SVSR boundary. A gap generally remains between the current approximation and the actual frontier of the statically secure operating region. The most informative unlabeled samples are therefore those located near this uncovered frontier, since their feasibility labels directly determine how the guaranteed region can be expanded.

Therefore, the proposed closed-loop active sampling strategy uses the current classifier to quantify the uncertainty of candidate terminal power profiles, prioritizes the most uncertain ones for numerical verification, and then updates the guaranteed region using the newly verified solvable samples. The updated region geometry is subsequently used to guide the next round of sampling. By repeating this process, the proposed method progressively improves the SVSR characterization with reduced computational effort.

IV. Case Study

To validate the proposed method, a five-terminal HVDC steady-state equivalent system is considered, as shown in Fig. 6. The system consists of two source terminals and three receiving-end load terminals interconnected through DC transmission branches, which provides a representative MT-HVDC testbed for SVSR characterization. The power-flow solvability check is performed in Python, where the feasibility of each candidate terminal-power profile is determined by an IPOPT-based solver. The overall learning procedure and result post-processing are implemented in Python and MATLAB.

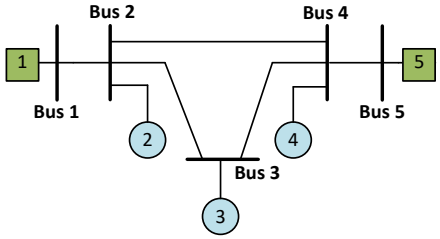


Fig. 6. Equivalent DC Topology of a Five-Terminal HVDC Test System, which Consists of Two Source Terminals and Three Receiving-End Load Terminals Interconnected through DC Transmission Branches.

Because the considered five-node MT-HVDC system contains three receiving-end power-injection terminals, the corresponding SVSR is naturally defined in a three-dimensional terminal-power space. Therefore, instead of presenting a two-dimensional slice, this paper directly reports the characterization results in the three-dimensional space spanned by the three terminal power injections. The classifier is implemented using a multi-layer perceptron (MLP) with one input layer, four hidden layers, and one output layer, and is trained using the ReLU activation function and the Adam optimizer. Within the proposed closed-loop framework, the current SVSR approximation is iteratively updated, and the most informative terminal power profiles are actively recommended for subsequent numerical verification.

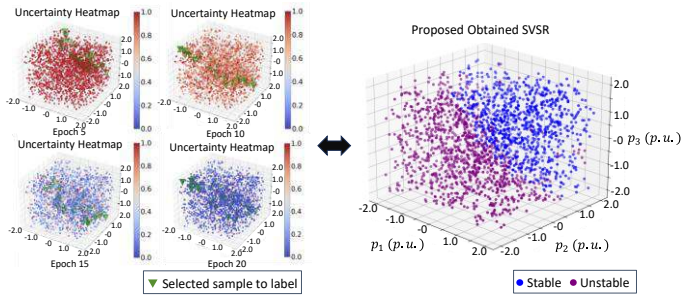


Fig. 7. SVSR characterization results for the five-terminal HVDC system. Left: representative snapshots of the proposed closed-loop active sampling process, showing uncertainty maps and queried samples selected for numerical verification. Right: final three-dimensional stable/unstable characterization in the terminal-power space obtained from the identified SVSR boundary. The proposed method attains an F1 score of 0.98 at epoch 18.

Fig. 7 illustrates the SVSR characterization results for the five-node MT-HVDC system. The left panel shows the evolution of the closed-loop active sampling process through representative uncertainty-map snapshots, together with the queried samples selected for labeling. It can be observed that, as the iterations proceed, the queried samples gradually concentrate around the informative transition region of the terminal-power space, indicating that the proposed method effectively focuses numerical effort on boundary-relevant operating conditions. The right panel shows the final three-dimensional stability characterization result obtained from the identified SVSR boundary, where stable and unstable operating points are separated in the terminal-power space. The proposed method reaches an F1 score of 0.98 at epoch 18, demonstrating that the main geometric features of the SVSR can be captured with high accuracy after a limited number of closed-loop refinement steps.

We further compare the computational efficiency of the proposed method against a conventional machine-learning (ML)-based baseline. For a fair comparison, both methods are tested on the same three-dimensional SVSR characterization task for the five-node MT-HVDC system, and the stopping criterion is defined as the time required to first reach an F1 score of 0.98. The results are summarized in Table I. The proposed approach reaches the prescribed accuracy threshold in 27 s on average, whereas the ML baseline requires 51 s. These results confirm that the proposed closed-loop active sampling framework can achieve accurate SVSR characterization for the five-node MT-HVDC system with substantially reduced computational effort.

TABLE I. Average Runtime for Reaching an F1 Score of 0.98 in Three-Dimensional SVSR Characterization of the Five-Terminal HVDC System

Run times	Proposed (s)	Machine learning (s)
1	30	52
2	28	51
3	26	51
4	25	52
5	26	51
Average	27	51

Overall, the case study on the five-terminal HVDC system yields two main findings. First, the proposed method provides an accurate characterization of the SVSR boundary. Second, compared with the conventional ML baseline, it reaches the target F1 score faster, highlighting its superior computational efficiency for MT-HVDC SVSR characterization.

V. Conclusions

This paper proposed a closed-loop active sampling method for SVSR characterization in MT-HVDC systems. By exploiting the steady-state equivalent DC-network model, the method combines interval-based subset construction, convex-subset expansion, and uncertainty-guided sample selection to progressively refine a guaranteed inner approximation of the SVSR. In this way, computational effort is concentrated on the most informative terminal power profiles rather than exhaustive random exploration. Case studies on a five-terminal HVDC system showed that the proposed method can accurately recover the main geometric features of the SVSR boundary. In addition, compared with a conventional ML-based baseline, the proposed approach reached an F1 score of 0.98 with substantially less computation time. These results demonstrate that the proposed framework provides an accurate and computationally efficient tool for SVSR characterization in MT-HVDC systems. Future work will extend the method to higher-dimensional terminal-power spaces, more complex MT-HVDC topologies, and online security assessment and control applications in hybrid AC/DC systems.

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